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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No. 500.38902X00

First Inventor or Application Identifier Takeshi SHIBUYA

Title See 1 in Addendum

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ * Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☒ Specification [Total Pages 29]
(preferred arrangement set forth below)
 - Descriptive title of the Invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to Microfiche Appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 8]
4. Oath or Declaration [Total Pages 5]
 - a. ☒ Newly executed (original or copy)
 - b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
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Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

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5. ☐ Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
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ACCOMPANYING APPLICATION PARTS

7. ☒ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement (when there is an assignee) ☒ Power of Attorney
9. ☐ English Translation Document (if applicable)
10. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. ☐ * Small Entity Statement(s) ☐ Statement filed in prior application Status still proper and desired (PTO/SB/09-12)
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Attachment to PTO/SB/05 (4/98) Utility Patent Application
Transmittal

1. HALFTONE PROCESSING APPARATUS USING DISTRIBUTING PWM METHOD
2. - FIGS. 1-3,4A-4H,5-12
- CREDIT CARD PAYMENT FORM
- Info. Discl. Sheet Under 37 CFR 1.56 w/refs.

HALFTONE PROCESSING APPARATUS USING
DISTRIBUTING PWM METHOD

BACKGROUND OF THE INVENTION

The present invention relates generally to an image output apparatus for printing an image produced by a printer, a facsimile or the like as a set of
5 points (pixels), and more particularly, to an apparatus for performing image processing to represent a continuous halftone image in combination of a laser pulse width modulation (PWM) with a clustered-dot dither screening method.

10 Conventionally, an increase in the number of tone levels in halftone images produced by a laser printer has often relied on a method of subdividing each one pixel by means of laser pulse width modulation (PWM).

15 However, a reduced width of a laser pulse often results in variations in resulting products, particularly in the charging characteristics of a photoconductor and a toner, and in higher susceptibility to instabilities due to environmental
20 variations such as temperature and humidity, thereby causing a problem of instable halftone reproduction in a highlight area, in which the image density is low, and a failure in providing a tone density commensurate with the number of divided laser pulses due to delayed
25 activation of the laser and a delayed response of the

photoconductor.

As a prior art approach addressing such problems, an article entitled "New Halftone Screening Technology Focused on Highlight Image Reproduction" (Japan Hardcopy '95 Transactions, pp. 143-146, by Yasuhiro Oda et al.) discloses a method of avoiding the use of narrow laser pulses by switching the halftone processing from line screen method to clustered-dot dither screen method only in a highlight area. JP-A-9-331448 discloses a method of stabilizing a reproduced image by adding adjustments to PWM outputs, using a look up table (LUT), corresponding to variations in environmental conditions and so on. Further, USP 5,134,495 (corresponding to Published Japanese Translation of PCT International Publication for Patent Application No. JP-A-6-504004) discloses a technology of performing a resolution transformation for increasing the resolution of a laser printer beyond the inherent engine performance by the use of multiple exposure of laser light which does not exceed a pixel threshold value.

Among the prior art approaches mentioned above, the method of processing a highlight area as clustered-dot dither screen is effective in stabilizing the reproduction of the tone in the highlight area, but may cause coarse isolated clustered-dot to be emphasized when a printer engine inherently has a large minimum pixel, leading to prominence of noise in the

highlight area.

Also, when a look up table is relied on to perform a feedback to the varying environment and aging changes, as disclosed in JP-A-9-331448, a large look up
5 table must be prepared or any interpolation means for continuously supporting the varying environment must be used in combination in order to finely respond to the varying environment. Otherwise, this method would emphasize instable images at boundaries at which one
10 look up table is switched to another. Of course, simple modifications of PWM output values using look up tables without performing the feedback with respect to the environmental conditions would not present characteristic differences from the γ -correction which
15 has been conventionally performed commonly on the halftone processing.

On the other hand, an instable region in a highlight area resulting from a shallow potential of an electrostatic latent image due to subdivided laser
20 pulses extends as an instable potential region increases near toner attaching limits in the latent image potential. Consequently, as such an instable region in the highlight area extends, the feedback correction using look up tables alone will experience
25 difficulties in achieving sufficient stability due to the influence of variations in individual photoconductor, the characteristic distribution on the particular photoconductor, and so on, in addition to

the influence of temperature and humidity. For this reason, the formation of a small, deep electrostatic potential to suppress the generation of instable potential regions plays a critical role for stabilizing
5 a highlight image quality.

However, a method relying on the resolution transformation as shown in USP 5,134,495 substantially requires pixel value information for interpolated pixels exceeding the device resolution, as it describes
10 "using a raster of pixels to represent said desired image, said raster having a predetermined raster resolution, said raster resolution being different from said device resolution." Thus, this type of method results in an increased cost of memories and associated
15 circuits, as well as a longer data transfer time.

In addition, even though the resolution transformation functions as an effective means for a high end machine which exhibits relatively stable characteristics in terms of the photoconductor and so
20 on, this is not true in low-price machines for use by general public, in which these characteristics are relatively instable, because the reproduction of isolated points is still instable as compared with dots of the inherent resolution originally provided by a
25 printer engine. Thus, the resolution transformation is not suitable for the reproduction of thin lines, and is only effective in a halftone representation in which a plurality of dots are grouped into a set, as is the

case with the clustered-dot dither processing, and in a relationship between clusters and dots as the smoothing of edges in fonts and so on.

It is therefore an object of the present
5 invention to provide an image processing apparatus for use also in low-price laser printers that may exhibit instable characteristics, which implements the halftone processing for stably increasing a concentration of highlight tone by simple circuits, which can be mounted
10 in ASIC, and accomplishes high speed and high quality image processing at a low cost.

SUMMARY OF THE INVENTION

The foregoing problem is solved by a halftone processing apparatus of the present invention, wherein
15 a plurality of pulse patterns including a pulse pattern which discretely divides one pixel and a pulse pattern which continuously divides one pixel are provided as PWM pulse patterns for subdividing one pixel originally produced by a printer engine, such that the discrete
20 pulse pattern and the continuous pulse pattern are switched by means of look up tables for a highlight area and another area, and this processing is combined with halftone processing relying on a clustered-dot dither for growing a plurality of clustered-dots in
25 cyclic manner.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a flow diagram illustrating the flow of data processing which includes the present invention;

5 Fig. 2 is a circuit diagram illustrating an example of a halftone processing apparatus according to the present invention;

Fig. 3 is a table showing a correspondence between input values and PWM pulse patterns;

10 Figs. 4A to 4H are diagrams showing a correspondence between PWM pulse patterns and printed dots;

Fig. 5 is a flow chart illustrating the operation of the tone processing apparatus;

15 Fig. 6 is a diagram illustrating an example of an input/output correspondence;

Fig. 7 is a diagram showing a method of composing a threshold value array from a basic threshold value pattern;

20 Fig. 8 is a table showing examples of basic threshold value patterns for realizing other screen angles;

Fig. 9 is a graph showing an example of γ -correction;

25 Fig. 10 is a block diagram illustrating another embodiment of the tone processing apparatus according to the present invention;

Fig. 11 is a block diagram illustrating a

further embodiment of the tone processing apparatus according to the present invention; and

Fig. 12 is a diagram illustrating an example of a color laser printer which is equipped with the tone processing apparatus according to the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

One embodiment of the present invention will hereinafter be described with reference to the accompanying drawings. Fig. 12 illustrates the configuration of a color laser printer 30 which contains a controller board 31 equipped with a halftone processing apparatus 9 to which the present invention is applied. In Fig. 12, the controller board 31 is represented by broken lines since it is mounted vertically on the bottom of the printer in parallel with other mechanisms required for printing operations. The tone processing apparatus 9 according to the present invention develops an input image signal in real time in synchronism with a horizontal synchronization signal and a vertical synchronization signal for controlling a photoconductive belt 32 and laser optics 33 to form an electrostatic latent image on the photoconductive belt 32.

It should be noted that while the following embodiment is described for color printing taken as an example, it goes without saying that the tone

processing apparatus according to the present invention can be applied to monochrome printing.

Fig. 1 illustrates the flow of image processing in a 600-dpi color printer which embodies the tone processing apparatus according to an embodiment of the present invention. Image data 1 to be printed is sent from a higher rank apparatus to the printer, and stored in an input buffer 2 as RGB data for one page. Since a printer engine 13 develops each of Y, M, C, K planes, the processing subsequent to the input buffer 2 in Fig. 1 is repeated four times, one for each of the Y, M, C, K planes, for one color image.

First, a four-color separating unit 5 initializes its interior as required to calculate Yellow from RGB point sequential data. In correspondence thereto, a γ -correction unit 7 loads an internal reference table with correction values corresponding to Yellow from a γ -correction value table 8. A dither circuit 10 in turn loads a threshold value array corresponding to Yellow and size data for the array from a table 11, and initializes its interior. The threshold value array is an array of values represented by eight bits in a range of 0 to 255 as shown in a threshold value array 27 of Fig. 8.

Thus, the RGB data sent from the input buffer 2 is subjected to a color correction by a color correction means 3, conversion to the Yellow data by the four color separating unit 5, and the tone

correction by the γ -correction unit 7, and then
outputted to the printer engine 13 as a PWM signal 12
by the tone processing apparatus 9.

As one page of the Yellow data has been
5 processed, the four-color separating unit 5, the γ -
correction unit 7, and the dither circuit 10 next
reload again required parameters for Magenta, and
initialize their interiors, respectively, and then
perform similar processing to send one page of PWM
10 signal 12 for Magenta to the printer engine 13.

Subsequently, the processing for Cyan and
Black is performed in a similar manner. The respective
color planes are switched in synchronism with the
vertical synchronization signal of the printer engine.
15 At this time, the threshold value array may be set such
that it is changeable for each color plane.

Next, an example of the tone processing
apparatus 9 is illustrated in Fig. 2. In the example
of Fig. 2, an input value n_i to the tone processing
20 apparatus 9 has 256 tone levels (represented by eight
bits), one dot is divided into four by PWM, and a
division pattern is specified by three bits.

Here, an OR circuit 15 and an OR circuit 35
in Fig. 2 are each a circuit which ORs the value of all
25 of four bits inputted thereto to output a 1-bit value
at "0" or "1" corresponding to the values, zero or non-
zero, of the four input bits. An OR circuit 16 in turn
ORs the value of each bit of a 5-bit input i_0 and a 1-

bit input i1 to output a 5-bit OR'ed value. Similarly, a NAND circuit 17 ANDs the value of each bit of the 5-bit input j0 and a negated 1-bit input j1 to output a 5-bit NAND'ed value.

5 In the former half of the processing in Fig. 2 including the NAND circuit 17, first, a difference Δn between a tone range of the input signal n_i and a dither threshold value n_c is calculated ($\Delta n = n_i - n_c$). Next, if the difference Δn is less than zero ($\Delta n < 0$), an
10 underflow signal from a subtractor circuit 14 causes the NAND circuit 17 to output all the bits at zero. On the other hand, if the difference Δn is equal to or larger than 16 ($\Delta n \geq 16$), the OR circuit 15 first outputs the four higher bits except for the underflow signal
15 from the subtractor circuit 14 at "1," and the OR circuit 16 outputs all the five bits at "1." Otherwise ($0 \leq \Delta n < 16$), the input 5-bit value to the OR circuit 16 is outputted as it is from the NAND circuit 17. These operations result in reduction of the 8-bit difference
20 Δn to a 5-bit value in a range of 0 to 15 (and all bits at "1" which represent 31 in decimal).

Next, subsequent to the NAND circuit 17, the 1-bit output of the OR circuit 35 is appended to the three higher bits of the NAND circuit 17 of the output
25 of the NAND circuit 17 as most significant side bit, and the two lower bits has been discarded, to produce a 4-bit value which is used as a selection signal for a PWM conversion table 22. Thus, the PWM conversion

table 22 selects and outputs a 4-bit PWM pulse pattern value in accordance with this selection signal.

Finally, a PWM generator circuit 23 outputs the pulse pattern value selected from the PWM conversion table 22 to the printer engine, as the final PWM signal.

In the foregoing description, of the 8-bit difference Δn , the three higher bits except for the underflow signal are discarded before the difference Δn is inputted to the OR circuit 16 to produce the 5-bit signal $i0$. However, the location at which the three higher bits are discarded in the circuit is not of particular importance. For example, the difference Δn may remain as an 8-bit signal until it passes through the NAND circuit 17, and after the difference Δn is outputted from the NAND circuit 17, the three higher bits and the two lower bits may be discarded from the 8-bit signal. Such implementation can also be readily made.

The next Fig. 3 shows an example of how the PWM conversion table 22 is set. An input value in the PWM conversion table 22 of Fig. 3 comprises the three lower bits as a first bit region determined by the difference value Δn and the most significant bit as a second bit region determined by the four higher bits of the threshold value n_c . The PWM conversion table 22 of Fig. 3 includes a PWM pulse pattern value column 22a which lists values having the second bit region set at "0" and a PWM pulse pattern value column 22b which

lists values having the second bit region set at "1."

Figs. 4A to 4H show a correspondence relationship between combinations of these pulse pattern values and dots which are printed in correspondence thereto. Particularly, Figs. 4A to 4H show growing patterns of isolated dots which discretely grow in response to the PWM pulse patterns. Specifically, in Figs. 4A to 4H, sequences of 0's and 1's separated every four digits on the upper stages 37a - 37h indicate pulse pattern values inputted to the PWM generator circuit; pulse patterns 38a - 38h on the middle stages show PWM signals outputted from the PWM generator circuit 23; and dot shapes 39a - 39h on the lower stages show the shapes of printed dots. It should be noted that in Figs. 4A to 4H, the respective signals are interpreted from left to right, and the corresponding dots 39a - 39h also grow from left to right.

In Figs. 4A to 4H, an original pulse for one dot of the printer engine is divided into four, so that the four-digit pulse pattern value corresponds to an ON/OFF pattern for one dot of the printer engine. In this event, as can be seen in Figs. 4A and 4B, in the formation of isolated dots, a dot 39a corresponding to a pulse pattern value 1010 is formed smaller than a dot 39b corresponding to a pulse pattern value 1100. Also, a dot 39c corresponding to a pulse pattern value 1101 is formed as a middle sized dot which is larger than

the dot 39b corresponding to the pulse pattern value 1100 and smaller than a dot 39d corresponding to a pulse pattern value 1110.

On the other hand, when an isolated dot is
5 corresponded to a pulse pattern value 1000, this leads to the formation of a lighter dot than the dot 39a corresponding to the pulse pattern value 1010, in which case the resulting image density is extremely low. Thus, such correspondence of the isolated dot to the
10 particular pulse pattern value results in an unnatural tone largely different in density from the dot 39b corresponding to the pulse pattern value 1100, as well as an instable image highly sensitive to the environment such as temperature, humidity and so on,
15 and to the influence of variations in components conditions of prienter engine.

Thus, by specifying the PWM pulse pattern value as shown in the table 22a of Fig. 3, the tone density effective to the isolated dots, which are
20 critical to the reproduction of a lower tone region, is increased twice as much as the prior art.

On the other hand, in a region in which a printed dot grows beyond one dot of the printer engine, as shown in Figs. 4E to 4H, the printed dots have grown
25 sufficiently large, so that a natural tone image can be ensured when the printed dots are produced in accordance with the table 22b of Fig. 3 rather than the table 22a. For this reason, the switching of pulse

patterns used when printed dots are isolated and those for other cases, as does in this embodiment, functions as an effective tone characteristic improving means.

The flow of the foregoing processing in Fig. 2 is next illustrated in a flow chart of Fig. 5. It should be noted that in Fig. 5, a PWM tone value p is used to refer to the first bit region (the three lower bits of the PWM tone value p in Fig. 2) to distinguish from the value s of the second bit region (the most significant bit of the PWM tone value p in Fig. 2).

The processing is performed in units of pages, i.e., for each color plane. First, at an initialization step 100 prior to the page processing, the PWM conversion tables 22a, 22b are loaded into a PWM correcting circuit 21.

At next step 101, an input pixel value n_i and a threshold value n_c are loaded, and at step 102, a difference Δn is calculated, and the four higher bits of the input pixel value n_i are set to s_1 . The threshold value n_c loaded at step 101 is sequentially inputted by the dither circuit 10 in Fig. 1 in synchronism with the input pixel value n_i based on a threshold value array 27 as shown in Fig. 7, later described, or a simplified threshold value array 28.

Next, at step 103, a PWM output value p is set to zero ($p=0$) when $\Delta n < 0$; to seven ($p=7$), i.e., 3 bits full or a maximum value represented by three bits, when $\Delta n \geq 16$; and to $\Delta n/4$ ($p=\Delta n/4$) when $0 < \Delta n < 16$. The

residue resulting from the division of Δn by four is discarded.

Then, this value p is used as an index at step 104a, where the output of a PWM correcting circuit 21a based on the PWM conversion table 22a is set to p' when $s1=0$, and at step 104b, where the output of a PWM correcting circuit 21b based on the PWM conversion table 22b is set to p' when $s1 \neq 0$.

Finally at step 105, the PWM generator circuit 23 outputs the PWM output level p' to the printer engine 13 as a pulse width modulated PWM signal.

The foregoing processing is repeated from step 101 until all pixels for one page have been processed, followed by the processing of Fig. 5 repeated from the beginning for the next page or the next color plane.

Next, Fig. 6 shows a correspondence relationship between the input tone value n_i and the threshold value n_c in the circuit of Fig. 2 and the PWM tone value p in the form of table. In Fig. 6, the input tone value n_i ($=0$ to 255) is represented in rows, and 4×10 sets of threshold values n_c ($=\{16k, 16k+1, 16k+2, 16k+3\}$, ($k=0, 1, 2, \dots, 9$)) are represented in columns. Also, examples of arrangement of threshold values in sets corresponding to Fig. 6 are shown in threshold value arrays 27 in Fig. 8, later described.

Specifically, in Fig. 6, the PWM tone value p

corresponding to the input tone value n_i from 0 to 3 is 0 or 8, each of which corresponds to the pulse pattern "0000" as derived from Fig. 3, so that the tone representation is identical for the input tone value n_i from 0 to 3. Thus, the number of logical output tone levels produced by combinations of 40 threshold values in Fig. 6 amounts to 161.

Next, Fig. 7 shows a method of constructing a threshold value array for implementing distributed processing for divided PWM in combination with the tone processing apparatus 9 illustrated in Fig. 2.

Assume first that a basic threshold value pattern 25 is K , and a threshold value interval Δh is 16. From K , an extended threshold value pattern 26 is constructed by four threshold value patterns produced by $K \cdot \Delta h$, $K \cdot \Delta h + 1$, $K \cdot \Delta h + 2$, $K \cdot \Delta h + 3$. Next, the extended threshold value patterns 26 are filled in a rectangular region which has periodically closed row and column to produce a threshold value array 27 as shown in Fig. 7.

The dither circuit 10 periodically and repetitively uses this threshold value array 27 to generate the threshold value n_c . The threshold value array 27 is constructed in such a manner that a set of two rows are stacked ten times downwardly while each set is shifted to the leftmost from the position indicated by an arrow A (the sixth column). It is therefore possible to employ a simplified threshold value array 28 formed of the upper two rows, instead of the entire threshold

value array 27, such that the two rows are repetitively used in synchronism with the horizontal synchronization signal of the printer engine 13, as the initial column address is shifted by six columns for every two rows of an input image, to save the capacity of memory required for the implementation of the present invention.

Also, in the example of Fig. 7, "1" and "2" may be replaced in the arrangement of the basic threshold value pattern 25 to construct the threshold value array. In this case, printed dots outputted corresponding to "1" in the basic threshold value pattern 25 are desirably outputted in accordance with the PWM pulse patterns associated with the second bit region set at "1" in Fig. 3 in a manner similar to printed dots which are outputted corresponding to "0" in the basic threshold value pattern 25.

Such a modification can be readily supported by changing the input to the OR circuit 35 of Fig. 2 to receive the three higher bits of the threshold value array nc.

The foregoing threshold value array 27 outputs clustered-dot lattices at an angle of approximately 18.4 degrees with respect to the horizontal direction for the intermediate uniform input tone values (e.g., $n_i=128$), as indicated by circles in Fig. 7. The angle formed by the clustered-dot lattice to the horizontal direction is referred to as the "screen angle." In general color printing, a

different screen angle is used for each color plane for purposes of stabilizing reproduced colors.

Next, Fig. 8 lists, in the form of table, examples of basic threshold value patterns K corresponding to a variety of screen angles θ . The values in the table has the following relationship:

$$(\text{total number of tone levels}) = (\text{number of cells}) \times \Delta h + 1 \text{ (here, } \Delta h=16 \text{)}.$$

As an example of assigning these threshold value patterns to the respective colors for color printing, when the pattern shown in Fig. 7 is assigned to Cyan; a pattern shown in Fig. 8(a) to Magenta; a pattern shown in Fig. 8(b) to Yellow; and a pattern shown in Fig. 8(c) to Black, moire due to overlapping of clustered-dot is less conspicuous in a resulting reproduced image. Of course, the patterns assigned to Magenta and Cyan may be reversed.

Fig. 8(d) shows an exemplary threshold value pattern in favor of the concentration of the clustered-dot, while Fig. 8(e) shows an exemplary threshold value pattern in favor of the halftone performance. In Fig. 8(e), however, when different values are assigned to respective cells in the basic threshold value pattern, the total number of tones exceeds 256, so that some of threshold values assigned to the respective cells in the basic threshold value pattern are repeated to limit the number of tones in the basic threshold value pattern to 16 (17 if including "0" tone), whereby the

total number of tones is limited to 256.

Conversely, the exemplary threshold value patterns shown in Figs. 8(a) to 8(d) have the total number of tones less than 256. In this case, when the
5 input tone value exceeds the total number of tones n_{max} plus 3, output dots are all set to ON, thus causing collapse in a higher tone region, as will be also inferred from Fig. 6. In such a situation, a γ -correction value provided to the γ -correction unit
10 before the tone processing apparatus 9 is limited to a value which prevents the input tone value from exceeding the total number of tones n_{max} to readily correct the collapse, as shown in Fig. 9.

In the example of Fig. 9, the γ -correction
15 value is entirely offset by approximately +3 in order to prevent the collapse even for the input tone value n_i from 0 to 3 in a highlight area.

While the foregoing embodiment provides the simplest implementation, a more flexible circuit
20 configuration is also possible provided that a slightly complicated implementation is not problematic. The next Fig. 10 illustrates an example which can produce similar effects to those of Fig. 2 even when the number of PWM stages is not a power of two. First, in
25 comparison with Fig. 2, description is made on functions which are added to Fig. 10 and which are modified from those of Fig. 2. The OR circuit 15 for performing the overflow processing in Fig. 2

corresponds to a comparator circuit 44 in Fig. 10. The OR circuit 15 in Fig. 2 outputs an overflow signal 1 when Δn 16, while a comparator circuit 44 in Fig. 10 outputs an overflow signal 1 based on a value Δh previously set in a register 40 when Δn Δh . As a result, an output from an AND circuit 17 in Fig. 10 is limited to zero or more and Δh or less, or to the value represented by all bits set at "1."

In Fig. 2, for the output from the NAND circuit 17, the two lower bits are consistently discarded, whereas in the example of Fig. 10, discard of the two lower bits and discard of the least significant bit can be selected by a selector circuit 46 in accordance with a value previously set in a register 41.

Assuming that the number of discarded lower bits of the output from the NAND circuit 17 is s , 2^s corresponds to the number of clustered-dots which distribute the tone level, as previously shown in the example of Fig. 7. The example of Fig. 7 shows the dither pattern which grows while circulating over four ($=2^2$) clustered-dots corresponding to the number of truncated bits ($s=2$). In addition, when $s=1$, it is readily inferred to construct a dither pattern which alternately grows between two ($=2^1$) clustered-dots. For this dither pattern, for example, assuming $\Delta h = (\text{number of PWM stages}) \times 2^s$, the pattern of $\Delta h \cdot K + 2$ may be replaced with the pattern of $\Delta h \cdot K$, and the

pattern of $\Delta h \cdot K + 3$ may be replaced with the pattern of $\Delta h \cdot K + 1$ in the extended threshold value pattern 26 of Fig. 7.

Also, the OR circuit 35 in Fig. 2 outputs "1" only when nc 16, which is used as the most significant bit of the selection signal for switching the address in the PWM conversion table 22. In Fig. 10, on the other hand, a comparator circuit 45 and a selector circuit 47 are used to add a value previously set in a register 43 to a selection signal 49 as an address offset which is added by an adder circuit 53 for selecting a PWM pulse pattern value in the PWM conversion table, only when nc 0 for the threshold value 0 previously set in a register 42.

With the modifications described above, the circuit illustrated in Fig. 10 performs the same operation as that of Fig. 2 when the value (Δh) in the register 40 is set to 16; the value in the register 41 to 0; the value (θ) in the register 42 is set to 16; and the value (p_0) in the register 43 to 8.

Other than the foregoing settings, in the circuit illustrated in Fig. 10, when the value (Δh) in the register 40 is set to 24; the value in the register 41 to 0; the value (θ) in the register 42 is set to 24; and the value (p_0) in the register 43 to 7, the number of PWM stages can be set to 6, the number of distributed mesh points can be set to 4, and so on. A dither threshold values adapted to this case can be

readily built by changing a multiplier Δh multiplied by the basic threshold value pattern K to 24 in the method of constructing a threshold value array shown in Fig. 7.

5 Next, Fig. 11 illustrates another exemplary implementation. Specifically, Fig. 11 shows an example in which the value (0) set in the register 42 is compared with a tone value n_i of an input pixel. In this case as well, the same effects as those of Fig. 10
10 can be produced in the example of Fig. 11. Further, in Fig. 11, lower bits of an output from a NAND circuit 17 are not simply discarded, but are added to upper bits as a carry-over by an OR circuit 50 and adder circuits 51, 52.

15 With this processing, an input/output correspondence relationship shown in Fig. 6 for the settings corresponding to the aforementioned Fig. 2 (when set as $\Delta h=16$, $s=0$, $\theta=16$, $po=8$) is equivalent to a relationship which shifts Fig. 6 by three rows, i.e., a
20 correspondence relationship which adds a constant integer 3 to the input tone value, so that the offset of +3, mentioned with respect to Fig. 9, can be eliminated.

 It is understood from the foregoing
25 description that, for example, in this case (when setting $\Delta h=16$, $s=0$, $\theta=16$, $po=8$ in Fig. 11), the PWM tone value p as an output signal from the selector circuit 46 is a value independent of the two lower bits of $\Delta n-3$

or $\Delta n+1$. It should be particularly noted that the nature of the effect of distributing PWM levels of clustered-dots growing by a combination with the threshold value pattern constructing method as shown in Fig. 7 is provided by the effect of discarding the lower bits of the difference Δn between the input tone value n_i and the threshold value n_c ($\Delta n = n_i - n_c$) (to which a constant is further added if necessary).

As described above, according to the present invention, the highlight tone concentration is stably improved by the PWM distribution processing, which is compatible with a clustered clustered-dot dither with a screen angle, and the divided PWM output patterns in a highlight area. Also, in the present invention, the foregoing effects can be realized by a small-scale circuit configuration, thereby facilitating the ASIC-based implementation of the stable halftone processing, which provides a higher resolution and a larger number of tone levels.

WHAT IS CLAIMED IS:

1. A halftone processing apparatus for a laser printer comprising:

a PWM circuit for controlling multi-level tone through laser pulse width modulation (PWM);

a threshold value array for converting a tone value (n_i) of an input pixel to a PWM tone value (p) based on a threshold value (n_c); and

a PWM correspondence table for associating a PWM tone value (p) to a corresponding laser pulse pattern, wherein:

said PWM tone value (p), when regarded as a bit sequence, comprises a first bit region which has a value determined depending only on a difference value ($\Delta n = n_i - n_c$) between said input tone value (n_i) and said threshold value (n_c), and a second bit region which has a value determined depending only on a value represented by said threshold value (n_c) excluding four or five lower bits thereof.

2. A halftone processing apparatus for a laser printer according to claim 1, wherein said PWM correspondence table associates some values of said first bit region of said PWM tone value (p) to a corresponding discontinuous pulse pattern as a laser pulse pattern corresponding to said PWM tone value (p) when the value (s_1) of said second bit region of said PWM tone value (p) is equal to zero ($s_1=0$); and to a corresponding continuous pulse pattern when said value

s1 is not equal to zero ($s1 \neq 0$), or to a corresponding discontinuous pulse pattern when said value s1 is not equal to zero ($s1 \neq 0$); and to a corresponding continuous pulse pattern when s1 is equal to zero ($s1 = 0$).

3. A halftone processing apparatus for a laser printer according to claim 1, wherein said first bit region of said PWM tone value (p) is determined for said difference value (Δn) and a certain constant integer (d) irrespective of the value represented by the two lower bits or the least significant bit of a value ($\Delta n + d$).

4. A halftone processing apparatus for a laser printer comprising:

a PWM circuit for controlling multi-level halftone through laser pulse width modulation (PWM);

a threshold value array for converting a tone value (n_i) of an input pixel to a PWM tone value (p) based on a threshold value (n_c); and

a PWM correspondence table for associating said PWM tone value (p) to a corresponding laser pulse pattern, wherein:

said tone processing apparatus further comprises:

registers for holding a threshold value (θ) and an address offset value (p_0); and

an adder circuit for adding said address offset value (p_0) to said PWM tone value (p), and

said PWM tone value (p) depends only on a

difference ($\Delta n = n_i - n_c$) between said input tone value (n_i) and said threshold value (n_c), and simultaneously, said address offset value (p_0) is switched on the basis of a comparison of said threshold value (n_c) with said threshold value (θ) or a comparison of said tone value (n_i) of said input pixel with said threshold value (θ).

5. A halftone processing apparatus for a laser printer according to claim 4, wherein said PWM correspondence table associates laser pulse patterns to some of said PWM tone values (p) such that one of a pulse pattern associated with said PWM tone value (p) and another pulse pattern associated with the sum of said PWM tone value and said address offset value ($p + p_0$) is a discontinuous pulse pattern and the other is a continuous pulse pattern, such that there is such a value p that one of p and $p + p_0$ is discontinuous and the other is continuous.

6. A halftone processing apparatus for a laser printer according to claim 5, wherein said PWM tone value (p) before said address offset value (p_0) is added thereto is determined for said difference value (Δn) and a suitable integer constant (d) irrespective of the value represented by the two lower bits or the least significant bit of a value ($\Delta n + d$).

7. A halftone processing apparatus for a laser printer according to claim 3, wherein said PWM tone value (p) for a uniform input sequentially increases as it circulates over four pixels, corresponding to an

increase in the value represented by the two lower bits of said input tone value (ni).

8. A halftone processing apparatus for a laser printer according to claim 3, wherein said laser printer is a color printer which performs multi-color printing through a plane sequential printing process for at least three colors, and comprises said threshold value array for each color plane to switch said threshold value arrays from one color plane to another.

9. A halftone processing apparatus for a laser printer according to claim 6, wherein said PWM tone value (p) for a uniform input sequentially increases as it circulates over four pixels, corresponding to an increase in the value represented by the two lower bits of said input tone value (ni).

10. A halftone processing apparatus for a laser printer according to claim 6, wherein said laser printer is a color printer which performs multi-color printing through a plane sequential printing process for at least three colors, and comprises said threshold value array for each color plane to switch said threshold value arrays from one color plane to another.

ABSTRACT OF THE DISCLOSURE

An image processing apparatus for a laser printer, wherein a halftone control through laser pulse modulation (PWM) is used in combination with distributed clustered-dot halftone processing which distributes a tone level over four clustered-dots, and the value represented by higher bits of a threshold are used to switch a PWM pulse pattern in a highlight area to a discontinuous pattern, thereby implementing the high density halftone processing, which provides a high highlight tone density and stability, only with a small scale memory and circuit.

FIG.1

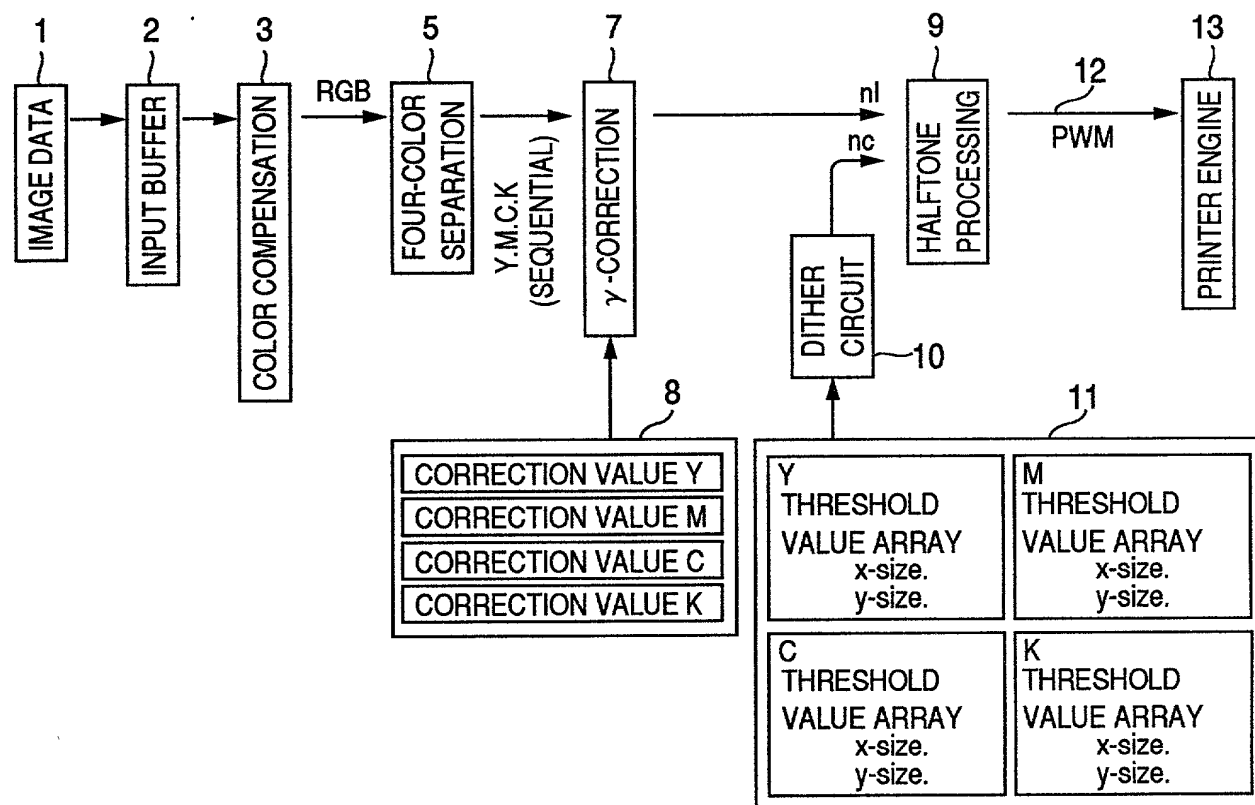


FIG.2

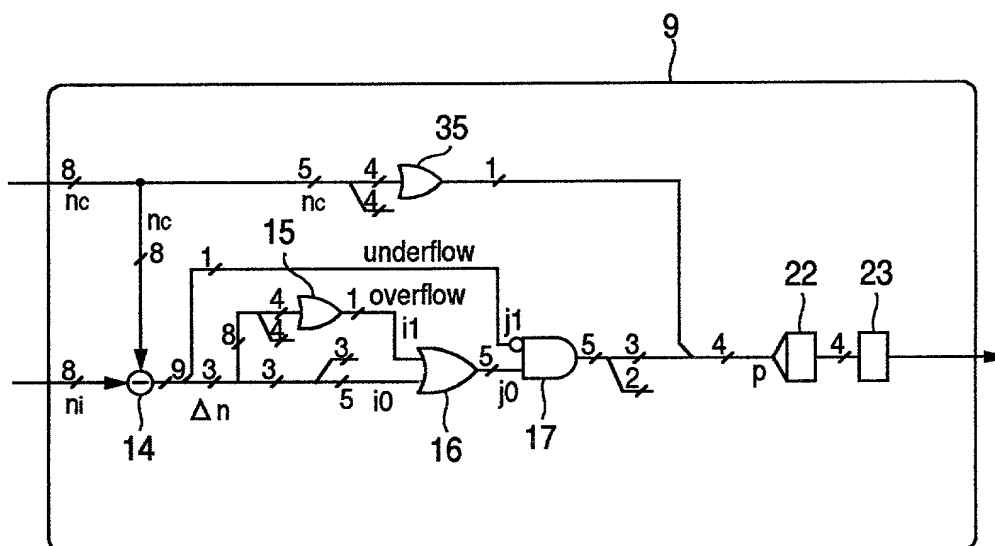


FIG.3

INPUT VALUE (BINARY)	PWM PULSE PATTERN VALUE	INPUT VALUE (BINARY)	PWM PULSE PATTERN VALUE
0000	0000	1000	0000
0001	1010	1001	1000
0010	1100	1010	1100
0011	1101	1011	1110
0111	1110	1111	1111

FIG.4A

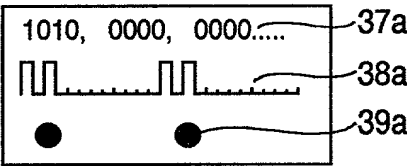


FIG.4E

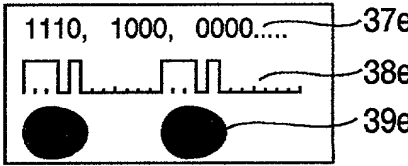


FIG.4B

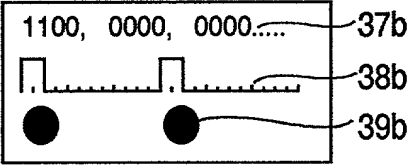


FIG.4F

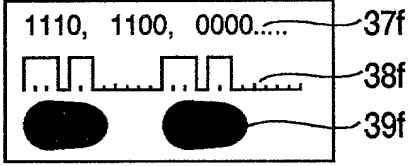


FIG.4C

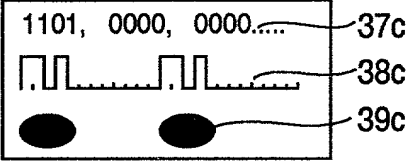


FIG.4G

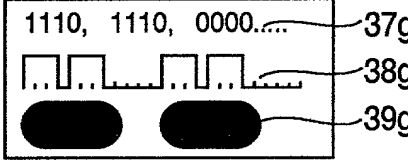


FIG.4D

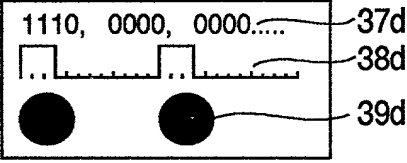


FIG.4H

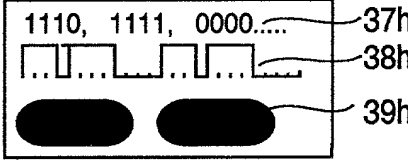


FIG.5

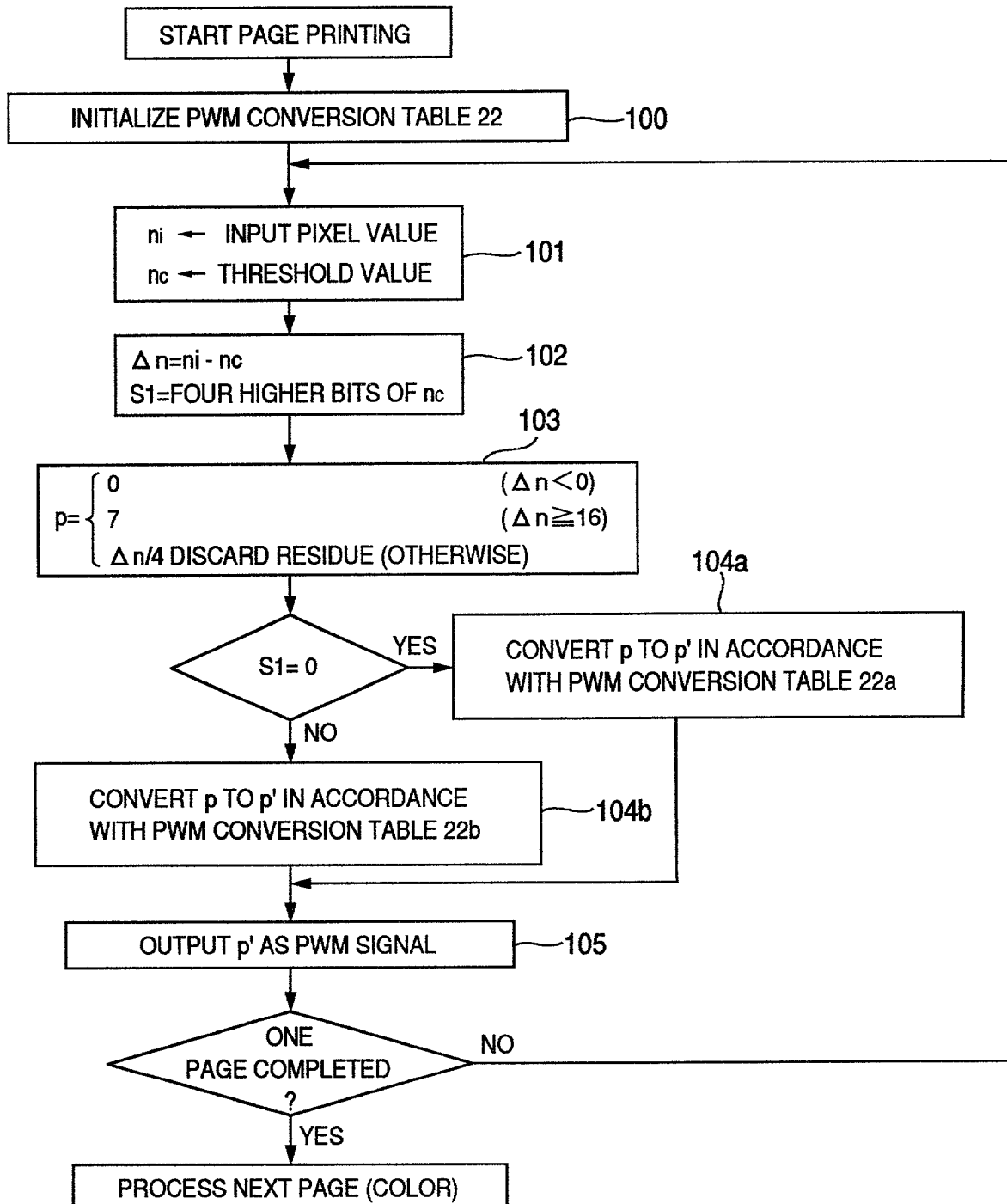


FIG.6

		THRESHOLD VALUE n_c																			
		0	1	2	3	16	17	18	19	32...	144...						147				
INPUT TONE VALUE n_i	n_c	0				1				2				3							
	k	0				1				2				3							
	0	0				8				8				8							
	1	0				8				8				8							
	2	0				8				8				8							
	3	0				8				8				8							
	4	0				8				8				8							
	5	0				8				8				8							
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	9	0				8				8				8							
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215																					

FIG.7

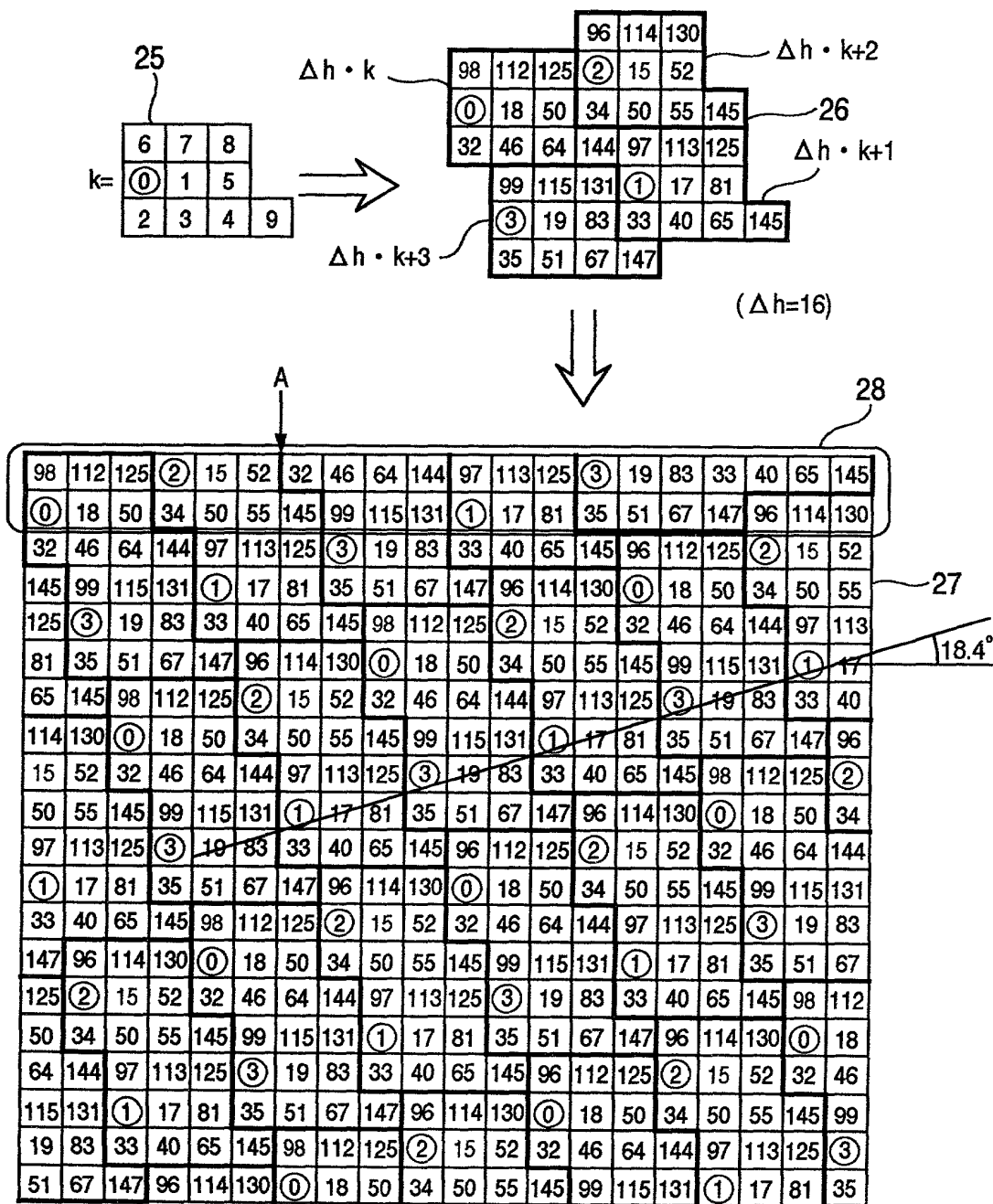


FIG.8

BASIC THRESHOLD VALUE PATTERN		θ	NUMBER OF CELLS	TOTAL NUMBER OF TONE LEVELS nmax																								
(a)	<table><tr><td>6</td><td>7</td><td>8</td><td>9</td></tr><tr><td>0</td><td>1</td><td>5</td><td></td></tr><tr><td>2</td><td>3</td><td>4</td><td></td></tr></table>	6	7	8	9	0	1	5		2	3	4		71.8°	10	161												
6	7	8	9																									
0	1	5																										
2	3	4																										
(b)	<table><tr><td>6</td><td>7</td><td>8</td></tr><tr><td>0</td><td>1</td><td>5</td></tr><tr><td>2</td><td>3</td><td>4</td></tr></table>	6	7	8	0	1	5	2	3	4	0°	9	145															
6	7	8																										
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(c)	<table><tr><td></td><td>5</td><td>6</td><td></td></tr><tr><td>7</td><td>0</td><td>1</td><td>4</td></tr><tr><td></td><td>2</td><td>3</td><td></td></tr></table>		5	6		7	0	1	4		2	3		45°	8	129												
	5	6																										
7	0	1	4																									
	2	3																										
(d)	<table><tr><td></td><td>0</td><td>1</td></tr><tr><td></td><td>2</td><td>3</td></tr><tr><td></td><td></td><td>4</td></tr></table>		0	1		2	3			4	26.5°	5	81															
	0	1																										
	2	3																										
		4																										
(e)	<table><tr><td>6</td><td>7</td><td>8</td><td>9</td></tr><tr><td>0</td><td>1</td><td>5</td><td>5</td></tr><tr><td>2</td><td>3</td><td>4</td><td>13</td></tr><tr><td>9</td><td>10</td><td>11</td><td>13</td></tr><tr><td></td><td></td><td></td><td>14</td></tr><tr><td></td><td></td><td></td><td>15</td></tr></table>	6	7	8	9	0	1	5	5	2	3	4	13	9	10	11	13				14				15	26.5°	20(15)	256
6	7	8	9																									
0	1	5	5																									
2	3	4	13																									
9	10	11	13																									
			14																									
			15																									

FIG.9

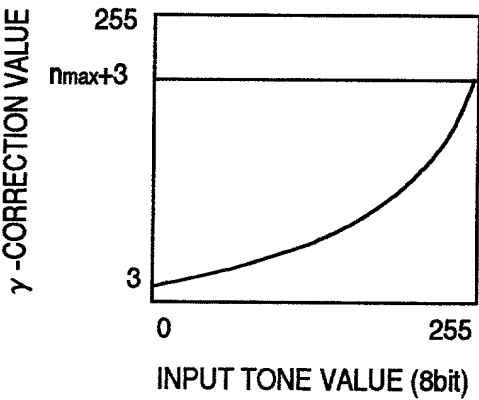


FIG.10

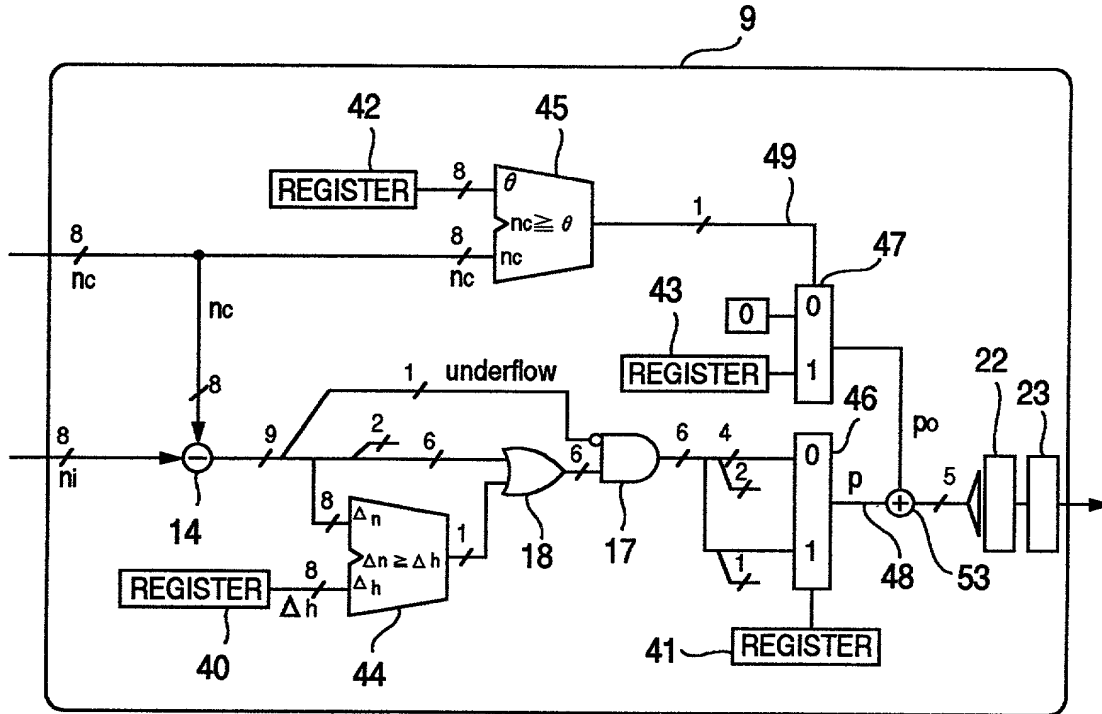


FIG.11

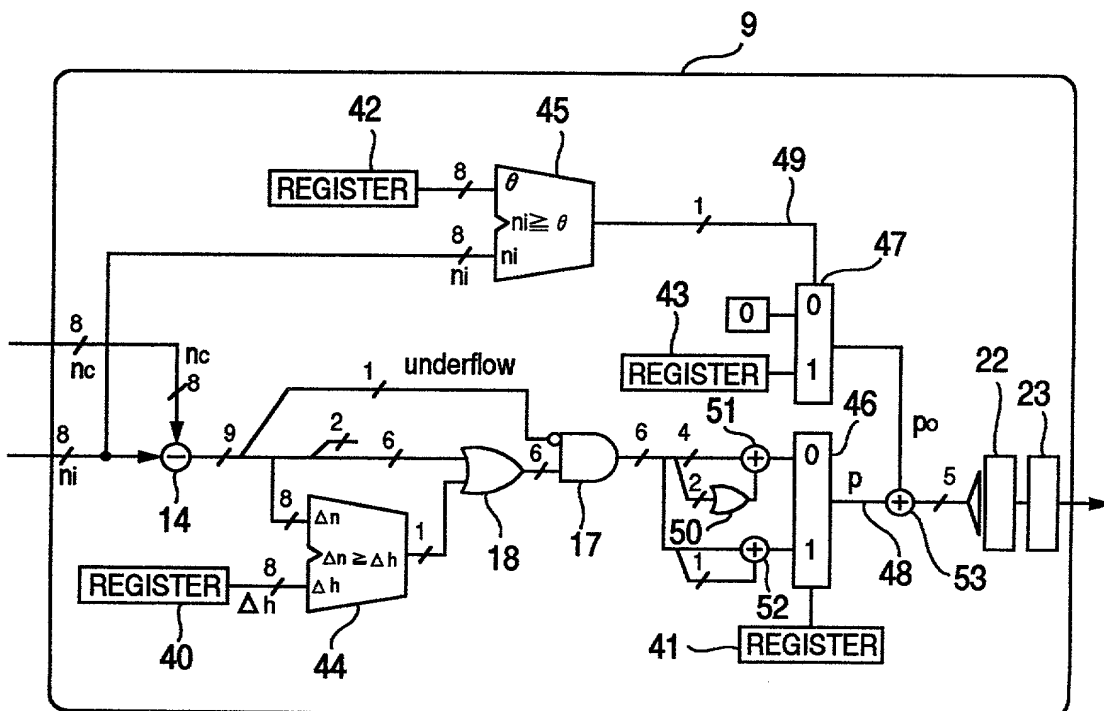
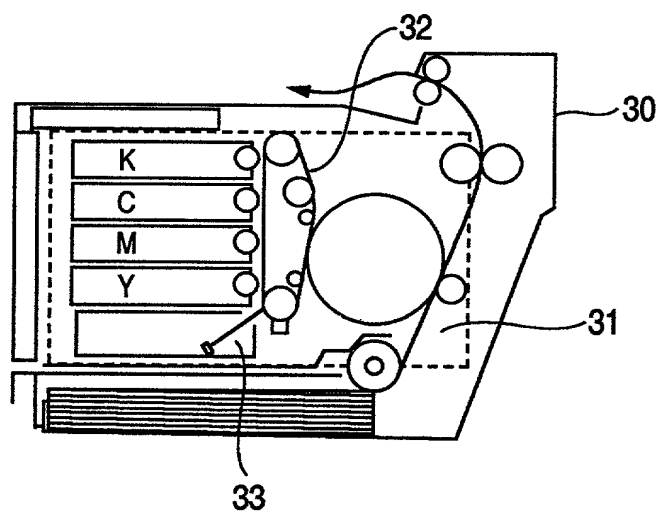


FIG.12



E5331-01

(*)

PTO/SB/106(8-96)

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Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"HALFTONE PROCESSING APPARATUS

USING DISTRIBUTING PWM METHOD"

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を____とし、
(該当する場合) _____に訂正されました。

☐ was filed on
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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Japanese Language Declaration (日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約365(a)項に基づき国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示している。

Prior Foreign Application(s)

外国での先行出願

11-271800 (Number) (番号)	Japan (Country) (国名)
(Number) (番号)	(Country) (国名)

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed
優先権主張なし

27/September/1999 (Day/Month/Year Filed) (出願年月日)	<input type="checkbox"/>
(Day/Month/Year Filed) (出願年月日)	<input type="checkbox"/>

私は、第35編米国法典119条(e)項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)
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(Application No.) (出願番号)	(Filing Date) (出願日)
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私は、下記の米国法典第35編120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づき権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)
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(Status: Patented, Pending, Abandoned) (現況: 特許許可済、係属中、放棄済)

(Application No.) (出願番号)	(Filing Date) (出願日)
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(Status: Patented, Pending, Abandoned) (現況: 特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じることに基づき表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行えば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

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(第二以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for second and subsequent joint inventors.)

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		Mieko ISHII	
第二共同発明者の署名	日付	Second inventor's signature	Date
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第四共同発明者		Full name of fourth joint inventor, if any	
第四共同発明者の署名	日付	Fourth inventor's signature	Date
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国籍	Citizenship		
私書箱	Post Office Address		
第五共同発明者		Full name of fifth joint inventor, if any	
第五共同発明者の署名	日付	Fifth inventor's signature	Date
住所	Residence		
国籍	Citizenship		
私書箱	Post Office Address		

(第六以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for sixth and subsequent joint inventors.)

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第六共同発明者		Full name of sixth joint inventor, if any	
第六共同発明者の署名	日付	Sixth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第七共同発明者		Full name of seventh joint inventor, if any	
第七共同発明者の署名	日付	Seventh inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第八共同発明者		Full name of eighth joint inventor, if any	
第八共同発明者の署名	日付	Eighth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第九共同発明者		Full name of ninth joint inventor, if any	
第九共同発明者の署名	日付	Ninth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	

(第十以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for tenth and subsequent joint inventors.)